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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,397	02/10/2004	Sohrab Kianian	2102397-992011	2419

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EXAMINER

THOMAS, TONIAE M

ART UNIT PAPER NUMBER

2822

DATE MAILED: 06/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/776,397

Applicant(s)

KIANIAN ET AL.

Examiner

Toniae M. Thomas

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2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 February 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 29-33,35-47 and 49-54 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 29-33,35-38,41-47 and 49-52 is/are rejected.
- 7) ☒ Claim(s) 39,40,53 and 54 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 10 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>02/10/04;10/12/04;02/14/05</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is a first Office action on the merits of Application Serial No. 10/776,397, which is a divisional of 09/982,413 filed on 17 October 2001, which will issue as US Patent No. 6,917,069 on 12 July 2005.
2. The preliminary amendment filed on 10 February 2005 cancelled claims 1-28, 34, and 48. Accordingly, claims 29-33, 35-47, and 49-54 are currently pending.

Specification

3. The specification is objected to because of the following informalities:
“now US Patent No. 6,917,069” should be inserted in the first line of the specification after “filed October 17, 2001.” Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 29-33, 35-38, 41-47, and 49-52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hofmann et al. (US 6,316,315 B1) in view of Wolf et al. (“Thermal Oxidation of Single

Crystal Silicon," *Silicon Processing for the VLSI Era - Vol. 1: Process Technology*).¹

The Hoffman et al. patent (Hofmann) discloses a method of forming an array of semiconductor memory cells (figs. 1-9 and accompanying text). The method comprises the steps of: forming a plurality of first regions, drains 45 (145), in a semiconductor substrate 20 that are substantially parallel to one another and extend in a first direction (fig. 1 and col. 5, lines 2-7; fig. 9 and col. 7, 62-67), wherein the substrate has a first conductivity type and the first regions have a second conductivity type (col. 4, lines 55-61); forming a plurality of trenches 53 into a surface of the semiconductor substrate (fig. 2 and col. 5, lines 23-29)², wherein the trenches are spaced apart from and extend substantially parallel to the first regions 45; forming a plurality of second regions, sources 60, in the substrate having the second conductivity type and are substantially parallel to one another, each of the second regions extends in the first direction and is formed underneath one of the trenches (fig. 2 and fig. 5, lines 29-32; col. 4, lines 55-61)³, wherein a plurality of channel regions 25 in the substrate are defined each having a first portion extending substantially along a sidewall of one of the trenches (fig. 7 and col. 7, lines 9-11) and a

¹ Applicant submitted the Hofmann et al. patent as prior art (see the 10 February 2004).

² The cross sectional views of figs. 1-8 show only one trench. However, it is clear from the plurality of memory cells shown in fig. 9 that Hofmann teaches forming a plurality of trenches 53 in the substrate.

³ The cross sectional views of figs. 1-8 show only one region 60 (source). However, it is clear from the plurality of memory cells shown in fig. 9 that Hofmann teaches forming a plurality of second regions 60 in the substrate.

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second portion that extends substantially along the substrate surface between the one trench and one of the first regions 45 (fig. 1 and col. 4, lines 55-58; fig. 2 and col. 5, lines 23-29); forming a plurality of floating gates 40 of electrically conductive material each disposed over and insulated from at least a portion of one of the channel regions 25 and a portion of one of the first regions 45 (figs. 1, 2; col. 4, line 65 - col. 5, line 2; col. 7, lines 16-21); forming a plurality of control gates 120 of electrically conductive material each having a first portion 140 disposed in one of the trenches (fig. 7 and col. 6, lines 53-64; col. 7, lines 20-27); and forming a layer of insulation material 115 between each of the floating gates and one of the control gates having a thickness permitting Fowler-Nordheim tunneling of charges there through (fig. 7 and col. 6, lines 46-55).

Spaced apart isolation regions 180 are formed on the semiconductor substrate, which are substantially parallel to one another and extend in a second direction substantially orthogonal to the first direction, with an active region between each pair of adjacent isolation regions; and insulating material is formed in portions of the trenches 170 that are in the isolation regions (fig. 9 and col. 4, lines 46-55).

The control gates 120 each have a second portion 130 disposed over and insulated from one of the floating gates (fig. 7 and col. 6, lines 60-62).

For each of the active regions, the control gate second portions 130 therein are electrically connected together (fig. 7).⁴

Each of the control gates forms a notch 150 at a connection between its control gate first portion 140 and its control gate second portion 130 (fig. 8 and col. 7, lines 1-8).

Each of the floating gates includes a sharp edge 105 that extends toward one of the notches (fig. 8 and col. 7, lines 1-8).

Each of the floating gates 40 is disposed over the entire second portion of one of the channel regions (fig. 2).

An insulating material 110, 115 is formed that extends along sidewalls of the trenches and between the control gates 120 and the floating gates 40 (fig. 7 and col. 6, lines 46-55).

Forming the insulating material 110, 115 includes the steps of: forming first portions 115 of the insulating material along sidewalls of the trenches and between the control gate first portions 140 and the channel region first portions (fig. 7 and col. lines 46-55); and forming second portions 110 of the insulating material under the control gate second portions 130 and over the floating gates 40 (figs. 6, 7 and col. 6, line 31).

Each of the channel region first portions extends in a direction directly toward one of the floating gates (fig. 7 and col. 7, lines 9-11).

⁴ See also the memory cell 150 of fig. 9.

The formation of the floating gates 40 includes forming a layer of the electrically conductive material 40 before the formation of the trenches 53, and wherein the trenches are subsequently formed through portions of the layer of electrically conductive material (figs. 1, 2; col. 4, line 65 - col. 5, line 2; and col. 5, lines 23-28).

As explained above, Hofmann discloses forming a layer of insulation material 115 between each of the floating gates and one of the control gates. The insulation layer is formed by thermal oxidation (col. 6, lines 46-55). While Hofmann discloses forming an insulation layer between each of the floating gates and one of the control gates, Hofmann does not disclose that the thermal oxide layer has a thickness permitting Fowler-Nordheim tunneling of charges there through. The Wolf et al. non-patent literature reference (Wolf), on the other hand, teaches that insulation layers formed by thermal oxidation have a thickness permitting Fowler-Nordheim tunneling of charges there through (see Table 1, page 198).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to form the insulation layer 115 of Hoffman such that its thickness permits Fowler-Nordheim tunneling of charges through the insulation layer, since insulation layers formed by thermal oxidation have a thickness that permits Fowler-Nordheim tunneling of charges through the insulation layer.

Allowable Subject Matter

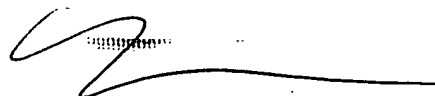
5. Claims 39, 40, 53, and 54 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. While Hofmann teaches forming indentations 150 (fig. 8 and col. 6, line 65 - col. 7, line 8), Hofmann does not anticipate, teach or suggest forming the indentations in a sidewall of each of the trenches 53 formed in the substrate. The prior art of record does not anticipate, teach or suggest a method of forming an array of semiconductor memory cells substantially as claimed, wherein the method comprises forming an indentation in a sidewall of each trench, as recited in claims 39 and 53.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Toniae M. Thomas whose telephone number is (571) 272-1846. The examiner can normally be reached on Monday through Friday from 8:30 a.m. to 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TMT
24 June 2004



Mary Wilczewski
Primary Examiner